**P2427**

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**Type of Project:** New IEEE Standard  
**PAR Request Date:** 07-Dec-2017  
**PAR Approval Date:** 15-Feb-2018  
**PAR Expiration Date:** 31-Dec-2022  
**Status:** PAR for a New IEEE Standard

1.1 **Project Number:** P2427  
1.2 **Type of Document:** Standard  
1.3 **Life Cycle:** Full Use

2.1 **Title:** Standard for Analog Defect Modeling and Coverage

3.1 **Working Group:** Analog Defect Coverage (C/TT/ACOVERAGE)  
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None

3.2 **Sponsoring Society and Committee:** IEEE Computer Society/Test Technology (C/TT)  
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None

4.1 **Type of Ballot:** Individual  
4.2 **Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot:** 03/2019  
4.3 **Projected Completion Date for Submittal to RevCom**  
**Note:** Usual minimum time between initial sponsor ballot and submission to Revcom is 6 months.: 10/2019

5.1 **Approximate number of people expected to be actively involved in the development of this project:** 40

5.2 **Scope:** This standard defines a defect coverage accounting method based on simulation models for defects observed within integrated circuits (ICs). The portion of all possible defects that are detected, or "covered", by tests of analog and mixed-signal circuits depends, in practice, on many factors (detectability, defect characteristics, detection threshold margin, measurement resolution, operating point, test patterns, etc.), which this standard considers as it defines how to report coverage.

This standard focuses on defects in analog functions. In this context, "defect" is an observable unintended physical change in a circuit, and an "analog function" means a function that has input, internal, or output signals with meaningful values in a defined continuous range, and the function has at least one parametric performance that is sufficiently non-deterministic that its test has upper and/or lower limits (the limits may be real numbers or quantized digital equivalents).

This standard considers redundancy, since most analog circuits have redundancy and defect tolerance, intentional or not. This standard does not consider combinations of variations that could result in a circuit failing to meet all its specifications - that is the subject of Monte Carlo simulations during design for yield and multi-parameter analog defect modeling.

The defects considered here are applicable to purely digital circuits too, though typically a simplified fault model (stuck-at, for instance) is utilized for digital functions. Thus, this standard assumes the topic of stuck-at fault coverage accounting is addressed for digital circuits by IEEE1804 "Standard for Fault Accounting and Coverage Reporting to Digital Modules."

5.3 **Is the completion of this standard dependent upon the completion of another standard:** No

5.4 **Purpose:** The primary purpose of this standard is to allow people to communicate information about defect coverage in a way that allows assessment of test and circuit quality as well as prediction of important metrics (simulation time, DfT circuit area, test time, test escapes, etc.).
Given a circuit description and a test pattern, this standard defines how to enumerate the universe of defects, determine which defects are detected by the test pattern, and report the coverage results.

By defining analog test coverage, this standard is useful for several other purposes.

First, this standard guides efficient simulation of defects to ensure that the defect models achieve a desirable trade-off between cost-effective simulation times and accurate modeling of behavior seen in real circuits.

Second, this standard facilitates estimation of test escape rates (historically measured in defective parts per million -- DPPM) to facilitate trade-offs between cost of test, time to market, and quality. The portion of all potential defects that tests must detect in a circuit will depend on the likelihood of the defects occurring, the consequences of undetected defects in the intended application for the IC, and the likelihood that a defect that occurs has a significant consequence.

Third, this standard facilitates improvements in design for test (DfT) and test generation methods. Many DfT and test techniques, including built-in self-test (BIST), have been developed which, despite cost advantages, are not used in practice because their impact on defect coverage is questioned due to the lack of a well-understood and silicon-corroborated analog defect model. By allowing reliable comparisons of DfT and test techniques, this standard facilitates automation and quality improvements.

5.5 Need for the Project: Unlike for digital circuits, the industry lacks a standardized way to specify the coverage of tests for analog and mixed-signal circuits. This omission has led to, at best, the use of incompatible ad hoc definitions or, at worst, no quantitative consideration of analog defect coverage at all. The anticipated benefits of using this standard include the following:

* Definition of a defect universe for a given analog circuit (schematic or layout netlist)
  - A list of defect types and their typical root causes
  - A practical, realistic model for each defect type
  - Equivalent defects that facilitate defect collapsing and simulating fewer defects
* Standard test coverage metrics for analog / mixed-signal circuits
  - A clear definition of defect detection criteria
  - A clear definition of defect coverage whereby different tools should give the same coverage for a given circuit and test
* Requirements for analog defect simulators; standard ways to automatically
  - Inject standard defects
  - Measure the ability of the tests to detect standard defects in circuit elements
  - List undetected defects
  - Report coverage of a circuit by a set of tests in an objective, traceable way
* A feedback mechanism (i.e., coverage measurement) that allows
  - Creation of higher coverage tests, for a defined set of defects (and likely others too)
  - Reduction of test time without reducing test coverage
* A more deterministic way to estimate DPPM for ICs containing analog circuitry
  - Based on defect coverage, accounting for defect clustering and defect likelihoods
  - Correlated to silicon DPPM
* A way to report in public papers, and internal reports, the coverage achieved by new test and DfT techniques, to allow more objective comparison to other approaches
* A basis for developing defect-oriented analog automatic test pattern generation (ATPG)
* Analog defect injection and simulation definitions/rules which could be extended to multi-parameter variation defects in the future.

5.6 Stakeholders for the Standard: Integrated-circuit (IC) designers, IC test engineers, IC suppliers, IC users.

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**Intellectual Property**

6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

7.1 Are there other standards or projects with a similar scope?: No
7.2 Joint Development
   Is it the intent to develop this document jointly with another organization?: No

8.1 Additional Explanatory Notes: