P2415

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Type of Project: New IEEE Standard
PAR Request Date: 25-Jun-2014
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PAR Expiration Date: 31-Dec-2018
Status: PAR for a New IEEE Standard

1.1 Project Number: P2415
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard for Unified Hardware Abstraction and Layer for Energy Proportional Electronic Systems

3.1 Working Group: UHA: Standard for Unified Hardware Abstraction and Layer (C/DA/UHA)
Contact Information for Working Group Chair
Name: Stanley Krolikoski
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None

3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)
Contact Information for Sponsor Chair
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None

4.1 Type of Ballot: Entity
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 12/2015
4.3 Projected Completion Date for Submittal to RevCom: 05/2016

5.1 Approximate number of entities expected to be actively involved in the development of this project: 10
5.2 Scope: The new standard defines the syntax and semantics for energy oriented description of hardware, software and power management for electronic systems. It enables specifying, modeling, verifying, designing, managing, testing and measuring the energy features of the device, covering both the pre- and post-silicon design flow. On the hardware side the description covers enumeration of semiconductor intellectual property components (System on Chip, board, device), memory map, bus structure, interrupt logic, clock and reset tree, operating states and points, state transitions, energy and power attributes; on the software side the description covers software activities and events, scenarios, external influences (including user input) and operational constraints; and on the power management side the description covers activity dependent energy control. The new standard is compatible with the current and future IEEE 1801 (UPF) standard to support an integrated design flow. It provides the higher level of abstraction and therefore enables earlier (more abstract) modeling of power states using UPF. Additionally, the new standard complements functional models in VHDL/Verilog/SystemVerilog/ SystemC by providing an abstraction of the design hierarchy and an abstraction of the design behavior with regard to power/energy usage.

5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: Current low power design and verification standard (IEEE 1801-2013 and IEEE P1801) is focused on the voltage distribution structure in design at Register Transfer Level (RTL) description and below. It has minimal abstraction for time (only interval function for modeling clock frequency), but depends on other hardware oriented standards to abstract events, scenarios, clock trees, etc. which are required for energy proportional design, verification, modeling and management of electronic systems. The necessary abstractions of hardware, as well as layers and interfaces in software are not yet defined by any existing standards. This standard addresses energy proportionality through tight interplay between energy-oriented hardware and energy-aware software. It provides new design, verification, modeling, management and testing abstractions and formats for hardware, software and systems to model energy proportionality, and enables the design methodology that naturally follows the top-down approach - from the system and software down to the hardware.

5.5 Need for the Project: The energy design and management flow for electronic devices is disconnected among different stages of the design

process and lacks the abstractions, formats, interfaces, and automated methodologies long established and standardized in functional design and verification of hardware and software for electronic systems. The main disconnects on energy issues are at the handover points between various design teams:
* From VLSI designers and IP providers to system integrators and power designers at the RTL level
* From system integrators to firmware developers at the core system software level
* From device developers and firmware developers to OS integrators at the OS API level
* From device developers and OS integrators to the application programmers at the application software level

The new standard has the goal to remove the above disconnects and lead to a well-connected energy oriented design flow enabling energy proportionality as the main design principle.

5.6 Stakeholders for the Standard: * Electronics systems designers (e.g., networking and mobile communications),
* Operating system and device driver developers,
* Embedded software and firmware developers,
* Software application developers,
* Device integrators,
* Processor providers (e.g., servers and laptops),
* Silicon vendors and manufacturers,
* Providers of semiconductor intellectual property (pre-designed blocks)
* Vendors of electronic design automation software

All of the above stakeholders have a vested interest in an industry standard for designing electronic systems with energy proportionality.

Intellectual Property
6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

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7.1 Are there other standards or projects with a similar scope?: No
7.2 Joint Development
Is it the intent to develop this document jointly with another organization?: No

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8.1 Additional Explanatory Notes (Item Number and Explanation): 5.2: UPF (Unified Power Format), VHDL (VHSIC Hardware Description Language), and VHSIC (Very High Speed Integrated Circuit)
5.5: VLSI (Very-large-scale integration), IP (Intellectual Property), OS (Operating System), and API (Application Program Interface)
1801-2013 - IEEE Standard for Design and Verification of Low-Power Integrated Circuits