P1804

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Type of Project: New IEEE Standard
PAR Request Date: 29-Jan-2009
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PAR Expiration Date: 31-Dec-2013
Status: PAR for a New IEEE Standard
Project Record: 1804

1.1 Project Number: P1804
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard for Fault Accounting and Coverage Reporting to Digital Modules (FACR)

3.1 Working Group: Fault Accounting and Coverage Reporting to Digital Modules (FACR) (C/TT/FACR 1804)
Contact Information for Working Group Chair
Name: Rajesh Raina
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None

3.2 Sponsoring Society and Committee: IEEE Computer Society/Test Technology (C/TT)
Contact Information for Sponsor Chair
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Contact Information for Standards Representative
None

4.1 Type of Ballot: Individual
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 02/2012
4.3 Projected Completion Date for Submittal to RevCom: 06/2012

5.1 Approximate number of people expected to be actively involved in the development of this project: 10
5.2 Scope: The standard formalizes aspects of fault models as they are relevant to the generation of test patterns for digital circuits. Its scope includes (i) fault counting (ii) fault classification, and (iii) fault coverage reporting across different ATPG (automatic test pattern generation) tools, for the single stuck-at fault model. With this standard, it will be incumbent on all ATPG tools (which comply to this standard) to report fault coverage in a uniform way, thereby facilitating the generation of a uniform coverage (and hence a test quality) metric for large chips with different cores and modules, for which test patterns have been independently generated.
5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: Digital circuits have various structural representations either in high level hardware description languages (HDLs) which can then be synthesised or in netlist forms. Commercial tools for automatic test pattern generation (ATPG) using algorithmic techniques today operate on a structural netlist of the design under test (DUT). The test quality signoff process mandatorily includes a minimal coverage requirement, to be obtained using these tool generated patterns on the DUT. This motivates the need for standard processes for (i) counting faults across different fault models, (ii) classifying these faults, and (iii) reporting the coverage, across different ATPG tools which are used to generate test patterns for these digital circuits. Such standard processes will make test qualification based on ATPG generated patterns and fault coverage metrics easier and independent of the ATPG tool used. A uniform fault coverage and pattern count based metric can now be generated for large chips with complex functionality which is being integrated into system-on-chips (SOCs) with a heterogeneous mix of modules therein, often consisting of Building Blocks (such as Intellectual Property (IP) cores - which are often sourced from design teams different from those designing the chips themselves), test patterns for which can be generated using different ATPG tools. (As the first step, only the classical stuck-at 0 and stuck-at 1 fault model will be considered. The fault accounting, classification and coverage reporting standard will be extended to cover other fault models subsequently).
5.5 Need for the Project: The standard will help to set uniform metrics for digital circuits with respect to their test quality in terms of coverage, as well as for different ATPG tools which are used to generate test patterns for these circuits.

5.6 Stakeholders for the Standard: All users of integrated electronic circuits, chips and chip-sets. ATPG tool developers and users.

Intellectual Property
6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board?: Yes
If yes, state date: 07-Nov-2008
6.1.b. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.c. Is the Sponsor aware of possible registration activity related to this project?: No

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7.1 Are there other standards or projects with a similar scope?: No
7.2 International Activities
a. Adoption
Is there potential for this standard (in part or in whole) to be adopted by another national, regional or international organization?: No
b. Joint Development
Is it the intent to develop this document jointly with another organization?: No
c. Harmonization
Are you aware of another organization that may be interested in portions of this document in their standardization development efforts?: No

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8.1 Additional Explanatory Notes (Item Number and Explanation): 3.1: P1804 Working Group Rajesh Raina (rajesh.raina@freescale.com) & Rubin Parekhji (parekhji@ti.com)