P1800

Submitter Email: karen_l_pieper@yahoo.com
Type of Project: Revision to IEEE Standard 1800-2012
PAR Request Date: 24-Nov-2015
PAR Approval Date: 05-Feb-2016
PAR Expiration Date: 31-Dec-2020
Status: PAR for a Revision to an existing IEEE Standard
Root Project: 1800-2012

1.1 Project Number: P1800
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language

Changes in title: ~~IEEE~~ Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language

3.1 Working Group: SystemVerilog Language Working Group (C/DA/1800_WG)
Contact Information for Working Group Chair
Name: Karen L Pieper
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Name: Neil Korpusik
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3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)
Contact Information for Sponsor Chair
Name: Stanley Krolikoski
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Contact Information for Standards Representative
None

4.1 Type of Ballot: Entity
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 10/2016
4.3 Projected Completion Date for Submittal to RevCom: 05/2017

5.1 Approximate number of entities expected to be actively involved in the development of this project: 8
5.2 Scope: This standard provides the definition of the language syntax and semantics for the IEEE 1800(TM) SystemVerilog language, which is a unified hardware design, specification, and verification language. The standard includes support for behavioral, register transfer level (RTL), and gate-level hardware descriptions; testbench, coverage, assertion, object-oriented, and constrained random constructs; and also provides application programming interfaces (APIs) to foreign programming languages.

5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: This standard develops the IEEE 1800 SystemVerilog language in order to meet the increasing usage of the language in specification, design, and verification of hardware. This revision corrects errors and clarifies aspects of the language definition in IEEE Std 1800-2012. This revision also provides enhanced features that ease design, improve verification, and enhance cross-language interactions.

Changes in purpose: This standard develops the IEEE 1800 SystemVerilog language in order to meet the increasing usage of the language in specification, design, and verification of hardware. This revision corrects errors and clarifies aspects of the language definition in IEEE Std 1800-~~2009~~2012.~~1~~ This revision also provides enhanced features that ease design, improve verification, and enhance cross-language interactions.

5.5 Need for the Project: With the ever increasing complexity of Very Large Scale Integrated Circuit design (VLSI) in the industry as driven by performance, functionality and power tradeoffs, the requirements for an enhanced, more powerful and extensive design language is also increasing. New designs include deeper pipelines, increased logic functionality, complexity, and power issues as well as explosion in the number of lines of Register Transfer Level (RTL) code as a result of the low abstraction level of the design supported by the existing languages. This has caused an increase, not only in design complexity, but also in the verification problem. Verification efforts are consuming

60% of the total design cycle and verification gets more challenging when multiple disciplines are used at different stages of the design. Examples of these disciplines are design specification, assertion based design, test bench based validation, coverage based specifications, and more. SystemVerilog was developed to enable the use of a unified language for abstract and detailed specification of the design, specification of assertions, coverage, and test bench verification that is based on manual or automatic methodologies. It also offers Application Programming Interfaces to provide access to information covered by the language. This standardization project will further develop the current IEEE standard for SystemVerilog in order to meet the increasing usage of the language as well as enabling consistent tool behavior from different vendors. The new revision of the standard will include resolutions and clarifications to errata and enhancements that will enable successful usage of the hardware design and verification language.

5.6 Stakeholders for the Standard: VLSI design and verification engineers and the Electronic Design Automation and Semiconductor Intellectual Property industry.

Intellectual Property
6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

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7.1 Are there other standards or projects with a similar scope?: Yes
If Yes please explain: IEEE Standards 1666, 1647, 1076, and 1850 all cover aspects of VLSI design and verification.

None of these standards utilize the Industry Standard syntax and semantics of SystemVerilog.

and answer the following
Sponsor Organization: DASC
Project/Standard Number: 1666, 1647, 1076, 1850
Project/Standard Date:
Project/Standard Title: 1076 (IEEE Standard VHDL Language)
1647 (IEEE Standard for the Functional Verification Language 'E')
1666 (IEEE Standard for Standard SystemC Language)
1850 (IEEE Standard for Property Specification Language)
7.2 Joint Development
Is it the intent to develop this document jointly with another organization?: No

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8.1 Additional Explanatory Notes (Item Number and Explanation): (In reference to item 5.5 above) the IEEE Std 1800-2012 is being revised to address errata, clarifications, and enhancements to support continued usefulness of the language in the design of large VLSI designs.