P1800

Submitter Email: karen_l_pieper@yahoo.com
Type of Project: Revision to IEEE Standard 1800-2009
PAR Request Date: 16-Apr-2010
PAR Approval Date: 17-Jun-2010
PAR Expiration Date: 31-Dec-2014
Status: PAR for a Revision to an existing IEEE Standard
Project Record: No Project Record
Root Project: 1800-2009   Edit Root Project Record

1.1 Project Number: P1800
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard for System Verilog--Unified Hardware Design, Specification, and Verification Language

3.1 Working Group: SystemVerilog Language Working Group (C/DA/1800_WG)
Contact Information for Working Group Chair
   Name: Karen Pieper
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   Name: Neil Korpusik
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3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)
Contact Information for Sponsor Chair
   Name: Stanley Krolikoski
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Contact Information for Standards Representative
   None

4.1 Type of Ballot: Entity
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 03/2012
4.3 Projected Completion Date for Submittal to RevCom: 10/2012

5.1 Approximate number of entities expected to be actively involved in the development of this project: 40
5.2 Scope: This standard provides the definition of the language syntax and semantics for the 1800 SystemVerilog language, which is a unified hardware design, specification, and verification language. The standard includes support for behavioral, register transfer level (RTL), and gate-level hardware descriptions; testbench, coverage, assertion, object-oriented, and constrained random constructs; and also provides application programming interfaces to foreign programming languages.

5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: This standard develops the 1800 SystemVerilog language in order to meet the increasing usage of the language in specification, design and verification of hardware. This revision corrects errors and clarifies aspects of the

Old Scope: This SystemVerilog standard (IEEE Std 1800) is a Unified Hardware Design, Specification, and Verification language. IEEE Std 1364TM-2005 Verilog is a design language. Both standards were approved by the IEEE-SASB in November 2005. This standard creates new revisions of the IEEE 1364 Verilog and IEEE 1800 SystemVerilog standards, which include errata fixes and resolutions, enhancements, enhanced assertion language, merger of Verilog Language Reference Manual (LRM) and SystemVerilog 1800 LRM into a single LRM, integration with Verilog-AMS, and ensures interoperability with other languages such as SystemC and VHDL.

Old Purpose: The purpose of this project is to provide the EDA, Semiconductor, and System Design communities with a solid and well-defined IEEE Unified Hardware Design, Specification and Verification standard language, while resolving errata and
language definition in the 1800-2009 standard. This revision also provides enhanced features that ease design, improve verification, and enhance cross language interactions.

5.5 Need for the Project: With the ever increasing complexity of Very Large Scale Integrated Circuit design (VLSI) in the industry as driven by performance, functionality and power tradeoffs, the requirements for an enhanced, more powerful and extensive design language is also increasing. New designs include deeper pipelines, increased logic functionality, complexity, and power issues as well as explosion in the number of lines of Register Transfer Level (RTL) code as a result of the low abstraction level of the design supported by the existing languages. This has caused an increase, not only in design complexity, but also in the verification problem. Verification efforts are consuming 60% of the total design cycle and verification gets more challenging when multiple disciplines are used at different stages of the design. Examples of these disciplines are design specification, assertion based design, test bench based validation, coverage based specifications, and more. SystemVerilog 1800 was developed to enable the use of a unified language for abstract and detailed specification of the design, specification of assertions, coverage, and test bench verification that is based on manual or automatic methodologies. It also offers Application Programming Interfaces to provide access to information covered by the language. This standardization project will further develop the current IEEE standard for SystemVerilog in order to meet the increasing usage of the language as well as enabling consistent tool behavior from different vendors. The new revision of the standard will include resolutions and clarifications to errata and enhancements that will enable successful usage of the hardware design and verification language.

5.6 Stakeholders for the Standard: VLSI design engineers and the EDA industry.

Intellectual Property

6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

7.1 Are there other standards or projects with a similar scope?: Yes
If Yes please explain: The scope of this PAR covers portions of the scope of previous PARs submitted by IEEE CS DASC. The existing PARs are: 1076, 1497, 1647, 1666, 1735, 1801, and 1850. The purpose of this PAR clearly states the intent to co-exist with the results of the standards produced by these working groups; to the best of our knowledge there are no impediments at this time to achieve the goal. In addition Accellera, Si2, and OSCI, all industry consortia within the EDA industry, have done work that covers the area of the scope of this PAR. OSCI with a SystemC environment, Accellera with OVL, an assertion language used in the verification of electronic circuit designs, and UCIS, a coverage unification standard, Verilog-AMS, a Verilog-based mixed signal design language, UVM, a universal verification methodology, and Si2 with CPF, the Common Power Format.

and answer the following

Sponsor Organization: IEEE CS DASC
Project/Standard Number: 1076, 1497, 1647, 1666, 1735, 1801, 1850
Project/Standard Date: 01-Apr-2010

7.2 International Activities
a. Adoption
Is there potential for this standard (in part or in whole) to be adopted by another national, regional or international organization?: Yes
Organization: International Electrotechnical Commission
Technical Committee Name: IEC TC93 WG2
Technical Committee Number: TC93
Contact Name: Dennis Brophy
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b. Joint Development
Is it the intent to develop this document jointly with another organization?: No
c. Harmonization
Are you aware of another organization that may be interested in portions of this document in their standardization
development efforts?: Yes
Organization: Accellera Organization, Inc.
Technical Committee Name: Verilog AMS
Technical Committee Number: 
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8.1 Additional Explanatory Notes (Item Number and Explanation):