myProject™ - P1734 PAR Detail

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Type of Project: New IEEE Standard

PAR Request Date: 15-Oct-2007

PAR Approval Date: 27-Mar-2008

PAR Expiration Date: 31-Dec-2012

PAR Signature Page on File: No

Status: PAR for a New IEEE Standard

Project: 1734

Root Project:

1.1 Project Number: P1734

1.2 Type of Document: Standard

1.3 Life Cycle: Full Use

1.4 Is this project in ballot now? No

2.1 Title: Standard for Quality of Electronic and Software Intellectual Property used in System and System on Chip (SoC) Designs

3.1 Working Group:

3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)

Contact Information for Sponsor Chair

Victor Berman
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Contact Information for Standards Representative

None

4.1 Type of Ballot: Entity

4.2 Expected Date of Submission for Initial Sponsor Ballot: 09/2008

4.3 Projected Completion Date for Submittal to RevCom: 04/2009

5.1 Approximate number of people expected to work on this project: 10

5.2 Scope: This specification defines a standard XML format for representing electronic IP quality information, based on an information model for electronic IP quality measurement. It includes a schema and the terms that are relevant for measuring electronic IP quality, including software that executes on the system. The schema and information model can be focused to represent particular categories of interest to IP users. In the context of this document, the term IP will be used to mean Intellectual Property electronic design data. Electronic Design Intellectual Property is a term used in the electronic design community. It refers to a reusable collection of design specifications which represent the behavior, properties, and/or representation of the design in various media.

5.3 Is the completion of this standard dependent upon the completion of another standard: No

5.4 Purpose: The purpose of this standard is to provide a unified view of quality measures for IP to facilitate the use and integration of this IP used in electronic system design. This will enable the continuous improvement of IP used for system design and verification by providing a mechanism for qualitative comparison between such IP. The standard IP quality measures and

characteristic exchange format defined can be incorporated into a variety of EDA tools.

5.5 Need for the Project: Faster product cycles and the more aggressive time-to-market requirements and more narrow market windows for new products, as well as limited resources in most companies doing chip design increases the motivation of chip designers to speed up their design process by reusing IP, especially in areas outside of the core competencies of the design teams. Quality issues in complex IP purchased from 3rd party providers in many cases end up seriously jeopardizing the timeliness of chip design completion and fabrication if the issues with the IP are found too late in the design process. Due to the high mask generation and fabrication costs of modern process nodes, an entire company may find itself at risk if a faulty IP is included in the design which results in non-functional chips and necessitates additional design, mask, and fabrication spending. Quality is the single most important issue hindering wide-spread IP adoption. A means for assessing the risk of IP which is being considered for use needs to be standardized. There are numerous ways and methodologies used to design and verify IP's resulting in a large variance in the quality of the IP. Adopting a quality standard metric that will account for the variances in designing, verifying and testing the IP will result in fair quality assessment and improved quality. The VSI Alliance is donating their Quality IP (QIP) metric to be used as a baseline for further development and wider adoption within IEEE ensuring a baseline by which all vendors measure and communicate quality aspects and facilitating more efficient IP evaluations and risk mitigation plans on the part of the IP consumer.

5.6 Stakeholders for the Standard: Stakeholders for this project include EDA vendors, IP vendors, electronic systems builders and IC manufacturers.

Intellectual Property

6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes
If yes, state date: 08/21/2007
6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? Yes
If yes, please explain: The standard will be based on material owned by the VSI Alliance. They have agreed to transfer the copyright of this material to the IEEE for use in this proposed standard.
6.1.c. Is the Sponsor aware of possible registration activity related to this project? No

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7.1 Are there other standards or projects with a similar scope? Yes
If yes, please explain:P1685 describes a method to handle IP that enables automated configuration and integration through plug-in tools. The proposed work describes a method to provide IP quality measures that are in addition and complimentary to the existing work. Another group that is looking at IP information exchange is IEEE Study Group P1735, specifically in the area of IP encryption.

and answer the following:
Sponsor Organization: DASC
Project/Standard Number: P1685 & P1735
Project/Standard Date: 08/11/2005
Project/Standard Title: Standard for IP-XACT, Standard Structure for Packaging, Integrating and Re-using IP within Tool-flows
Recommended Practice for Design Intellectual Property (IP) Encryption and Rights Management

7.2 Future Adoptions
Is there potential for this standard (in part or in whole) to be adopted by another national, regional, or international organization? Do not know at this time

7.3 Will this project result in any health, safety, security, or environmental guidance that affects or applies to human health or safety? No

7.4 Additional Explanatory Notes: (Item Number and Explanation)
