P1149.10

Submitter Email: cclark@intellitech.com
Type of Project: New IEEE Standard
PAR Request Date: 14-Jun-2013
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PAR Expiration Date: 31-Dec-2017
Status: PAR for a New IEEE Standard

1.1 Project Number: P1149.10
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: High Speed Test Access Port and On-chip Distribution Architecture

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3.1 Working Group: High Speed Test Access Port and On-chip Distribution Architecture (C/TT/HJTAG)
Contact Information for Working Group Chair
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None

3.2 Sponsoring Society and Committee: IEEE Computer Society/Test Technology (C/TT)
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None

4.1 Type of Ballot: Individual
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 06/2015
4.3 Projected Completion Date for Submittal to RevCom: 10/2015

5.1 Approximate number of people expected to be actively involved in the development of this project: 25
5.2 Scope: This standard defines a high speed test access port for delivery of test data, a packet format for describing the test payload and a distribution architecture for converting the test data to/from on-chip test structures.

The standard re-uses existing High Speed I/O (HSIO) known in the industry for the High-Speed Test Access Port. The HSIO connects to an on-chip distribution architecture through a common interface. The scope includes the distribution architecture test logic and packet decoder logic. The objective of the distribution architecture and packet decoder is that it can be readily re-used with different Integrated Circuits (ICs) that host different HSIO technology such that the standard addresses as large a part of the industry as possible.

The scope includes IEEE 1149.1 Boundary Scan Description Language (BSDL) and Procedural Description Language (PDL) documentation which can be used for configuring a mission mode HSIO to a test mode compatible with the High Speed Test Access Port (HSTAP). The same BSDL and PDL can then be used to deliver high-speed data to the on-chip test structures.

5.3 Is the completion of this standard dependent upon the completion of another standard: No
5.4 Purpose: This document will not include a purpose clause.
5.5 Need for the Project: Test time has always been an important metric for Systems on a Chip (SoCs). The original 1149.1 test access port is fine for simple board interconnect but as on-chip operations via the 1149.1 Test Access Port (TAP) have increased it becomes inefficient for board test and on-board Field Programmable Gate Array (FPGA) configuration. Large FPGAs take tens of minutes to configure through the 1149.1 TAP. The 1149.1 TAP has always been too slow for production SoC test. Wide Test Access Mechanisms (TAMs) are used to increase test throughput during production IC test at the cost of requiring more tester resources. Wide TAMs are also not useful for test re-use at board/system since many I/O are not accessible. A High-Speed Test Access Port and distribution matrix is needed by the industry to standardize a faster test data delivery mechanism for the IC Automatic Test Equipment (ATE) but also can be re-used at the board and system. This mechanism can transfer data for test, debug or FPGA configuration.

5.6 Stakeholders for the Standard: IC manufacturers, FPGA manufacturers, Test Equipment providers.

Intellectual Property
6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

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7.1 Are there other standards or projects with a similar scope?: No
7.2 Joint Development
Is it the intent to develop this document jointly with another organization?: No

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8.1 Additional Explanatory Notes (Item Number and Explanation): none at this time