myProject™ - P1149.1 PAR Detail

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Type of Project: Revision to IEEE Standard

PAR Request Date: 24-May-2008

PAR Approval Date: 26-Sep-2008

PAR Expiration Date: 31-Dec-2012

Status: Revision to an Existing IEEE Standard 1149.1-2001

Root PAR: P1149.1 **Approved on:** 26-Jun-1997

Project Record:

1.1 Project Number: P1149.1

1.2 Type of Document: Standard

1.3 Life Cycle: Full Use

2.1 Title: Standard Test Access Port and Boundary Scan Architecture

Old Title: Standard Test Access Port and Boundary Scan Architecture

3.1 Working Group:

3.2 Sponsoring Society and Committee: IEEE Computer Society/Test Technology (C/TT)
Contact Information for Sponsor Chair
Name: Rohit Kapur
Email: rkapur@synopsys.com
Phone: 1
Contact Information for Standards Representative
None

4.1 Type of Ballot: Individual

4.2 Expected Date of Submission for Initial Sponsor Ballot: 09/2008

4.3 Projected Completion Date for Submittal to RevCom: 03/2009

5.1 Approximate number of people expected to work on this project: 22

5.2 Scope: This standard defines test logic that can be included in an integrated circuit
to provide standardized approaches to
- testing the interconnections between integrated circuits once they have been
assembled onto a printed circuit board or other substrate;
- testing the integrated circuit itself; and
- observing or modifying circuit activity during the component's normal operation.
The test logic consists of a boundary-scan register and other building blocks and
is accessed through a Test Access Port (TAP).

Old Scope: Corrections, clarifications and enhancements of IEEE Std 1149.1a and Std. 1149.1b. Combine these two standards into one document.

5.3 Is the completion of this standard dependent upon the completion of another standard: No

5.4 Purpose: 1.2.1 An overview of the operation of IEEE Std 1149.1

This subclause provides a general overview of the operation of a component compatible with this standard
and provides a background to the detailed discussion in later subclauses.

The circuitry defined by this standard allows test instructions and associated test data to be fed into a
component and, subsequently, allows the results of execution of such instructions to be read out. All
information (instructions, test data, and test results) is communicated in a serial format.

The sequence of operations would be controlled by a bus master, which could be either an automatic test
equipment (ATE) or a component that interfaces to a higher-level test bus as a part of a complete system
maintenance architecture. Control is achieved through signals applied to the Test Mode Select (TMS) and
Test Clock (TCK) inputs of the various components connected to the bus master. Starting from an initial
state in which the test circuitry defined by this standard is inactive, a typical sequence of operations would
be as follows.

The first steps would be, in general, to load serially into the component the instruction binary code for the
particular operation to be performed. The test logic defined by this standard is designed such that the serial
movement of instruction information is not apparent to those circuit blocks whose operation is controlled by
the instruction. The instruction applied to these blocks changes only on completion of the shifting (instruction
load) process.

Once the instruction has been loaded, the selected test circuitry is configured to respond. In some cases,
however, it is necessary to load data into the selected test circuitry before a meaningful response can be
made. Such data is loaded into the component serially in a manner analogous to the process used previously
to load the instruction. Note that the movement of test data has no effect on the instruction present in the test

Old Purpose As technology has changed, the original 1149.1 standard does not address the new needs of the end users. The purpose of this PAR is to address these new needs in the IEEE 1149.1 standard. The intended users are silicon vendors, silicon designers, board and system electronic manufacturers and test equiment manufacturers. The benefits are additional capabilities and ease-of-use of 1149.1 for the current technology of mix-signal devices, differential logic and programmable devices.

circuitry.
After execution of the test instruction, based where necessary on supplied data, the results of the test can be
examined by shifting data out of the component to or through the bus master. Note that in cases where the same test operation is to be repeated but with different data, new test data can be
shifted into the component while the test results are shifted out. There is no need for the instruction to be
reloaded.
Operation of the test circuitry may proceed by loading and executing several further instructions in a manner
similar to that described and would conclude by returning the test circuitry and, where required, on-chip
system circuitry to its initial state.
1.2.2 The use of IEEE Std 1149.1 to test an assembled product
This subclause outlines the use of the boundary-scan circuitry defined by this standard during the process of
testing an assembled product such as a printed circuit board.
The test problem for any product constructed from a collection of components can be decomposed into three
goals:
a) To confirm that each component performs its required function;
b) To confirm that the components are interconnected in the correct manner; and
c) To confirm that the components in the product interact correctly and that the product performs its
intended function.
This approach can be applied to a board constructed from integrated circuits, to a system constructed from
printed circuit boards, or to a complex integrated circuit constructed from a set of simpler functional
modules. To simplify the discussion, this description henceforth will concentrate on the case of an
assembled printed circuit board constructed from a collection of digital integrated circuits.
At the board level, goal a) and goal b) typically are achieved by using in-circuit test techniques; for goal c),
a functional test is required. However, in-circuit test techniques have significant limitations when viewed
against evolving surface-mount interconnection technology, for example, the

difficulty of making reliable contact to miniaturized features of the printed circuit board using a bed-of-nails fixture. How, then, might the above three test goals be achieved if test access becomes limited to the normal circuit connections, plus a relatively small number of special-purpose test connections?

Considering goal a), it is clear that the vendor of an integrated circuit used in the board-level design will have an established test methodology for that component. The components could be tested on a proprietary ATE system or by using a self-test procedure embedded in the design. Information on the test methodology adopted is typically not available to the component purchaser. Even where self-test modes of operation are known to exist, they may not be documented and therefore are not available to the component user.

Alternative sources of test data for the board test engineer may be the component test libraries supplied with in-circuit test systems or the test programs developed by component users for incoming inspection of delivered devices.

Wherever the test data for a component originates, the next step is to use it once the component has been assembled onto the printed circuit board. If access is limited to the normal connections of the assembled circuit, this task may be far from simple. This is particularly true if the surrounding components are complex or if the board designer has tied some of the components connections to fixed logic levels or has left component pins unconnected. Normally, it will not be possible to test the component in the same way that it was tested in isolation unless an in-circuit test is achievable.

To ensure that built-in test facilities can be used or that preexisting test patterns can be applied, a framework is needed that can be used to convey test data to or from the boundaries of individual components so that they can be tested as if they were freestanding. This framework will also allow access to and control of builtin test facilities of components. Boundary scan

coupled with a test access bus provides such a framework.

The objective of this standard is to define a boundary-scan architecture that can be adopted as a standard feature of integrated circuit designs, thus allowing the required test framework to be created on assembled printed circuit boards and other products.

1.2.3 What is boundary scan?

The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan register cell) adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles.

Figure 1-1 illustrates an example implementation for a boundary-scan register cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can be either loaded into the scan register from the Signal-in port (e.g., the input pin) or driven from the register through the Signal-out port of the cell (e.g., into the core of the component design).

As will be discussed in detail in Clause 11, the second flip-flop (controlled by input Clock B) is provided to ensure that the signals driven out of the cell in the latter case are held while new data is shifted into the cell using input Clock A. This flip-flop is not required in all cases but is included in Figure 1-1 to simplify the discussion.

The boundary-scan register cells for the pins of a component are interconnected to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and appropriate clock and control signals. Within a product assembled from several integrated circuits the boundary-scan registers for the individual components could be connected in series to form a single path through the complete design, as illustrated in Figure 1-2. Alternatively, a board design could contain several independent boundary-scan paths.

If all the components used to construct a circuit have a boundary-scan register, the resulting serial path through the complete design can be used in

two ways:
a) To allow the interconnections between the various components to be tested, test data can be shifted into all the boundary-scan register cells associated with component output pins and loaded in parallel through the component interconnections into those cells associated with input pins; and
b) To allow the components on the board to be tested, the boundary-scan register can be used as a means of isolating on-chip system logic from stimuli received from surrounding components while an internal self-test is performed.
Alternatively, if the boundary-scan register is suitably designed, it can permit a limited slow-speed static test of the on-chip system logic since it allows delivery of test data to the component and examination of the test results.
These tests allow the first two goals discussed earlier to be achieved through the use of the boundary-scan register. In effect, tests applied using the register can detect many of the faults that in-circuit testers currently address, but without the need for extensive bed-of-nails access. The third goal to functionally test the operation of the complete product remains and can be achieved either by using a functional (through the pins) ATE system or by using a system-level self-test, for example.
Note also that by parallel loading the cells at both the inputs and outputs of a component and shifting out the results, the boundary-scan register provides a means of sampling the data flowing through a component without interfering with the behavior of the component or the assembled board. This mode of operation is valuable for design debugging and fault diagnosis since it permits examination of connections not normally accessible to the test system.

1.2.4 The use of IEEE Std 1149.1 to achieve other test goals

In addition to its application in testing printed circuit assemblies and other products containing multiple components, the test logic defined by this standard can be used to provide access to a wide range of design-for-test features built

into the components themselves. Such features might include internal scan paths, selftest functions [e.g., using built-in logic block observer (BILBO) elements], or other support functions.
Design-for-test features such as these can be accessed and controlled using the data path between the serial
test data pins of the TAP defined by this standard. Instructions that cause internal reconfiguration of the
component's system logic such that the test operation is enabled may be shifted into the component through
the TAP.

5.5 Need for the Project: The need is to address feedback given by balloters during reaffirmation as well as address input from 1149.4/1149.6/P1687/P1149.7. These modfications will make it easier for designers to implement an IC with several of these standards incorporated as well as allow the IC to maintain compliance with each standard.
5.6 Stakeholders for the Standard: IC producers, PCB manufacturers and test equipment vendors.

Intellectual Property
6.1.a. Has the IEEE-SA policy on intellectual property been presented to those responsible for preparing/submitting this PAR prior to the PAR submittal to the IEEE-SA Standards Board? Yes
If yes, state date: 05/20/2008
6.1.b. Is the Sponsor aware of any copyright permissions needed for this project? No
6.1.c. Is the Sponsor aware of possible registration activity related to this project? No

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7.1 Are there other standards or projects with a similar scope? No

7.2 International Activities

a. Adoption
Is there potential for this standard (in part or in whole) to be adopted by another national, regional or international organization? Do Not Know
Organization:
Technical Committee Name:
Technical Committee Number:
Contact Person Name:
Contact Person Phone:
Contact Person Email:

b. Joint Development
Is it the intent to develop this document jointly with another organization? No

c. Harmonization
Are you aware of another organization that may be interested in portions of this document in their standardization development efforts? No

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8.1 Additional Explanatory Notes (Item Number and Explanation): The title, scope and purpose as currently written in IEEE 1149.1 will not be modified under this PAR. The scope of this activity is to address feedback given during the reaffirmation, address input given by 1149.4/1149.6. Changes will be made to enable other proposed standards such as P1687, P1149.7 and related efforts to use the standard more effectively. IEEE P1149.7 is Standard for Reduced-pin and Enhanced-functionality Test Access Port and Boundary Scan Architecture. IEEE 1149.6 is IEEE Standard for Boundary-Scan Testing of Advanced Digital Networks. IEEE P1687 is Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device. IEEE 1149.4 is standard for mixed signal test bus. The Purpose section contains two figures, Figure 1-1 A boundary-scan register cell and Figure 1-2 A boundary-scannable board design, which we not able to be copied and pasted to this PAR form. 3.1 Working Group Information:

Standard Test Access and Boundary Scan Architecture WG P1149.1, Contact: CJ Clark, cjclark@intellitech.com, Phone: 603-868-7116 3.2: Rohit Kapur's phone number is 650-584-1487
