P1076

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Type of Project: Revision to IEEE Standard 1076-2008
PAR Request Date: 04-Feb-2011
PAR Approval Date: 31-Mar-2011
PAR Expiration Date: 31-Dec-2019
Status: PAR for a Revision to an existing IEEE Standard
Project Record: P1076
Root Project: 1076-2008

1.1 Project Number: P1076
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard for VHDL Language Reference Manual


3.1 Working Group: VHDL Analysis and Standardization Group (C/DA/P1076)

Contact Information for Working Group Chair
Name: Jim Lewis
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3.2 Sponsoring Society and Committee: IEEE Computer Society/Design Automation (C/DA)

Contact Information for Sponsor Chair
Name: Stanley Krolikoski
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Contact Information for Standards Representative
None

4.1 Type of Ballot: Individual
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 07/2014
4.3 Projected Completion Date for Submittal to RevCom

Note: Usual minimum time between initial sponsor ballot and submission to Revcom is 6 months.: 10/2014

5.1 Approximate number of people expected to be actively involved in the development of this project: 30

5.2 Scope: This standard defines the syntax and semantics of the VHDL Hardware Description Language (VHDL). The acronym, VHDL (Very High Speed Integrated Circuits), in the language’s name comes from the U.S. government program that funded early work on the standard.

Changes in scope: This standard revision defines the syntax and semantics of the VHDL-VHIC Hardware Description Language (VHDL). The acronym, VHIC (Very High Speed Circuit), in the language’s name comes from the U.S. government program that funded early work on the standard.

5.3 Is the completion of this standard dependent upon the completion of another standard: No

5.4 Purpose: VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Since it is both machine and human readable, it supports the design, development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and

Changes in purpose: The VHDL language is a formal notation intended for use in all design phases and of documentation the creation of electronic systems. Since it is both machine and human readable, it supports the language's design,
procurement of hardware.

This document is intended for the implementers of tools supporting the language and the advanced users of the language.

5.5 Need for the Project: General language enhancements improve designer productivity by allowing the specification of models more efficiently or the ability to specify functionality that was previously not possible or impractical to specify in VHDL. Verification capabilities are needed to improve the quality of the designs and to address the significant and growing portion of the electronic system design schedule that is being spent in ensuring the design is functionally correct before manufacturing. These capabilities directly address productivity and quality.

5.6 Stakeholders for the Standard: - Digital IC and FPGA IP developers
- Digital IC and FPGA developers and manufacturers
- Digital and embedded system developers, manufacturers and integrators,
- Electronics Design Automation (EDA) tool vendors

Intellectual Property
6.1.a. Is the Sponsor aware of any copyright permissions needed for this project?: No
6.1.b. Is the Sponsor aware of possible registration activity related to this project?: No

7.1 Are there other standards or projects with a similar scope?: Yes
If Yes please explain: There are three other projects with a similar scope: IEEE 1647 (e), IEEE 1800 (System Verilog), IEEE 1850 PSL. There is overlap between the capabilities of these languages/ However, VHDL has been proven in the market and multiple tools currently support it.

cf. section 8.1 for additional details.

and answer the following

Sponsor Organization: IEEE Design Automation Standards Committee (DASC)
Project/Standard Number: 1800
Project/Standard Date: 11-Dec-2009

7.2 Joint Development
Is it the intent to develop this document jointly with another organization?: No

8.1 Additional Explanatory Notes: For section 7.1, there are two other standards or projects beside P1800 with a similar scope, viz., P1647 and P1850. The information for these is

Sponsor Organization: IEEE/DASC
Project/Standard Number: P1647
Project/Standard Date: 05/09/2008
Project/Standard Title: IEEE Standard for the Functional Verification Language e

Sponsor Organization: IEEE/DASC
Project/Standard Number: P1850
Project/Standard Date: 03/25/2010
Project/Standard Title: IEEE Standard for Property Specification Language (PSL)